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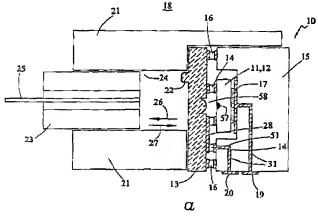
(54) Title: HERMETIC CHIP-SCALE PACKAGE FOR PHOTONIC DEVICES

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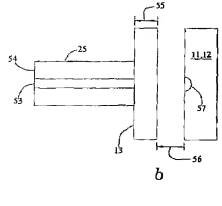


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(57) Abstract: A package having one or more integrated circuit photonic devices in a hermetically sealed enclosure. The photonic devices may be sources or detectors of light. The sealed enclosure consists of a transparent window attached to a first level housing. The transparent window contains patterned electrically conductive traces for purposes of routing electrical signals to and from semiconductor chip, which is bonded to patterned window. A second level housing is attached to the first level housing, and aligned via mechanical features incorporated with the transparent window. The second level housing provides a receptacle for a plug having light waveguides or optical fibers that are aligned with the photonic devices when inserted into the receptacle. One or more pins are inserted through the plug and the second level housing to secure the plug in the receptacle to the hermetically sealed photonic devices, such as VCSEL's on an integrated circuit semiconductor.

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— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

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# HERMETIC CHIP-SCALE PACKAGE FOR PHOTONIC DEVICES

## BACKGROUND

The Government may have rights in this invention pursuant to Contract No. F30602-97-2-0120, awarded by the Department of the Air Force.

Optical coupling and electrical connections to photonic devices, particularly arrays of them on a single chip, are subject to environmental effects, electrical parasitics, and mechanical misalignment. There appears to be no adequate packaging approaches available to effectively eliminate these problems and at the same time provide ruggedized, compact, high-performing and reliable systems.

## SUMMARY OF THE INVENTION

The invention is a hermetic packaging of optical emitters and/or detectors via bump bonding on an electrically patterned transparent window. It is to simultaneously provide sealed containment or hermeticity and optical coupling to VCSEL's or detectors, either in arrays or as single devices. These devices or device are

made of a semiconductor such as gallium arsenide. Hermeticity is often required for environmentally sensitive devices. No such hermetic array package is known.

The semiconductor is bump bonded to a window patterned with electrically conductive traces, which is itself sealed at the periphery to a ceramic or similar package. Electrical connections to, say, multi-layer impedance controlled traces external to the sealed cavity are accomplished within the ceramic package. The window may be equipped with refractive or diffractive lenses to improve optical coupling into and out-of the package. The optical devices and corresponding lenses may be in the form of one or two-dimensional arrays. Fibers being optically connected to an array of devices may be in the form of a ribbon or cord having a multitude of fibers for conveying light to or from the devices. Mechanical features are included to provide passive or semi-active alignment to a second level package that encompasses the first level package containing the optical devices. The package may be used in conjunction with an optical back plane. This approach provides precision optical coupling alignment, mechanical ruggedness, compactness, optical and electrical isolation, very low parasitics, high speed performance, protection from moisture, humidity and other dehabilitating

contaminants of the ambient environment, device reliability, and fabrication advantages.

## BRIEF DESCRIPTION OF THE DRAWING

Figure 1a shows a hermetic 1st-level package for optical devices and their optical and electrical couplings, both to board-level electrical pads and to optical fibers via the indicated 2nd-level package assembly.

Figure 1b provides a view of the optical coupling between optical fibers and a photonic device.

Figure 2a shows a window having metal traces and mechanical registration features formed on it.

Figure 2b reveals a housing having photonic devices, the electrical interconnects of which match up with the corresponding interconnects on the window.

Figures 3a and 3b illustrate a housing having a pin arrangement for connecting and securing a ferrule or plug having the optical light wave guides or fibers that are brought next to the window.

Figures 4a and 4b shows a perspective view of a plug and housing having the pin arrangement.

DESCRIPTION OF THE EMBODIMENTS

Figure 1a shows a hermetic chip scale package 10 for photonic devices. To attain hermeticity and efficient optical coupling to a linear or 2-dimensional array of VCSEL's 11 and/or detectors 12, the semiconductor die containing the VCSEL's or detectors is bump bonded to a partially metalized window 13 at electrically conductive bump 14. Window metallization 28 can be some combination Cr, Pt, Au, Ti, Cu, ITO, or Ni, either sputtered, evaporated, or plated. Window 13 is also sealed at the periphery to multi-layer ceramic package 15 with hermetic solder seal 16, while simultaneously completing chip-to-window electrical connection at conductive bump 14. Chip 11, 12 is attached to ceramic package 15 via electrical and/or thermal connection 17. Chip 11, 12 is hermetically sealed from an ambient environment 18 of device 10. Electrical connection 17 is connected to chip 11, 12 and to external pad 19 via conductive path 31. The pad at bump 14 is also connected to electrical path 31 via conductive trace 28 from chip 11, 12 to pad 51, and thereby to external electrical connection pad 20 via path 31. A refractive and/or diffractive optical element 58 may be etched into or deposited on a surface of the window to

facilitate improved optical coupling efficiency. The package, so far described, is a first level package.

A second level package is housing 21 and fits on and around the first level package encompassing chip 11, 12 within a hermetic seal. Housing 21 is mechanically aligned with one or more keys 22 on window 13. Ferrule 23 is inserted within housing 21 and may be slid into a position where an edge 24 of the ferrule buts up against key or keys 22. Situated in ferrule 23 is a fiber or fibers 25, which convey light signals 26 from VCSEL's 11, and/or light signals 27 to detectors 12. Housing 21 may be secured to the first level housing with glue, adhesive or an epoxy. Once ferrule 23 is inserted all the way into housing 21, it may or may not be glued into place.

Figure 1b shows a closer view of the optical coupling between fiber 25 and photonic device 11, 12. Light comes or goes through core 53 of fiber 25. Cladding 54 covers and protects glass core 53. Cladding has an index of refraction so as to contain the light within core 53. Fiber 25 butts up against window 13. Window 13 has a thickness 55 that ranges from roughly 25 to 250 microns. The index of refraction of the material of window 13 is about 1.52. That index may vary dependent on the particular design of package 10. Between window 13 and the

emanating or sensing portion 57 of device 11, 12, there is a gap 56 of about 25 microns.

Figure 2a shows window 13 onto which first level housing 15 is adhered via solder seals 16. Light signal source 11 or detector 12 is bump bonded to transparent window 13 via electrically conductive or metal traces 28 on the surface of window 13 and metal terminals 29 on chip 11, 12 with solder bumps 14. Metalization strips 28 may have lateral dimensions of 20 to 50 microns, and thicknesses of less than 5 microns. Chip 11, 12 is typically between 3 and 8 millimeters. Window 13 may be composed of a material such as quartz or sapphire. Solder ring 16 may be composed of tin in combination with lead, gold or silver. Solder bumps 14 may be composed of tin in combination with lead, gold or silver.

Figure 2b illustrates housing 15 having optical devices 11, 12 with electrical connecting spots 58 that match up with conductive strips 28 so as to electrically connect sensitive areas 57 of devices 11, 12 with connecting spots 29. External connections 20 are connected in housing 15 to connecting spots 29.

Figure 3a shows an embodiment 40, which utilizes a pin 42 to hold plug or ferrule 43 to housing 41. Figure 3a shows a cut-away section along pin 42. Figure 3b, on the

other hand, shows a cut-away section along fiber 25 and emanation or receptor area 57. Ferrule 43 has an edge 44 which is butted up against bumper 45, which may be an elastomeric seal, as shown in figure 3b. Pin 42 is inserted through an alignment hole 51 in ferrule 43 and alignment hole 52 in housing 41 and is secured in place with a retaining clip 46 inserted in notch 47 at the end of pin 42. Ferrule 43 is held firmly in place with the tension of a loading spring 48 between ferrule 43 and clip or shoulder 49 at the end of pin 42, which is opposite of the end having notch 47. Pin 42 and holes 51 and 52 provide a less than the plus or minus five micron alignment between fiber 25 and VCSEL 11 or detector 12 emanation or receptor area 57, respectively, as shown in figure 3b. Since ferrule 43 is not glued to housing 41, it may be removed whenever desired by removing clip 46 from notch 47. Chip 11, 12 according to embodiment 40 is hermetically sealed. However, one may choose to have chip 11, 12 not hermetically sealed by replacing the multi-layer ceramic package with an FR4 or equivalent plastic package in cost-reduced embodiment 40.

An arrangement, as shown in figures 4a and 4b, has one or more pins 42 holding a ferrule 43 with a fiber array 25 to housing 41. Pins 42 and respective holes 51 and 52 are

placed on each side of fiber array 25 for secure, robust and precision alignment of fiber array 25 with lens 37 and sensitive or emanating area 57 of chip 11, 12.

In another embodiment, plug or ferrule 43 may be part of a backplane, and housing 41 may be attached to an opto-component circuit board, which is plugged into the backplane via plug 43 and housing 41.

Other embodiments and variants of the present invention, not disclosed here, are covered by the claims and only limited in scope by the claims, which includes all equivalents thereof.

THE CLAIMS

1. A chip-scale package for photonic devices, comprising:

a window;

a chip fixed on said window; and

an enclosure formed over said chip and on said window.

2. The package of claim 1, wherein said chip is hermetically sealed by said window and enclosure.

3. The package of claim 2, wherein said cover is sealed to said window at the periphery of said window by a sealing-type material.

4. The package of claim 3, wherein said window has at least one conductive trace.

5. The package of claim 4, wherein said chip comprises a photonic device.

6. The package of claim 5, wherein said chip is connected to the at least one conductive trace.

7. The package of claim 6, further comprising a housing formed around said window.

8. The package of claim 7, further comprising a ferrule having at least one optical fiber, which is placed against the said window.

9. The package of claim 8, further comprising a lens formed on said window.

10. The package of claim 9, wherein said ferrule is plugged into an opening formed by said housing.

11. The package of claim 10, wherein the optical fiber is proximate to said window so that light from the fiber can go through the optical fiber and said window to photonic device, and so that light from the photonic device can go through said window and the least one optical fiber.

12. A chip-scale package for photonic devices, comprising:
a first housing;
a chip attached to said first housing; and
a window attached to said first housing.

13. The package of claim 12, further comprising:
at least one conductive trace formed on said window; and

the at least one conductive trace is connected to said chip and to a pad.

14. The package of claim 13, wherein said first housing and said window form a hermetically sealed volume containing said chip.

15. The package of claim 14, wherein the pad is situated externally relative to the sealed volume.

16. The package of claim 15, further comprising a second housing attached to said first housing.

17. The package of claim 16, wherein said chip has at least one photonic device.

18. The package of claim 17, further comprising a ferrule having at least one optical waveguide.

19. The package of claim 18, wherein said ferrule plugs into a portion of said second housing.

20. The package of claim 19, wherein the at least one optical waveguide becomes aligned with the at least one

photonic device when said ferrule is plugged into the portion of said second housing.

21. The package of claim 20, further comprising a pin for holding said ferrule in a plugged-in position in the portion of said second housing.

22. The package of claim 21, wherein said window has at least one lens situated between the at least one photonic device and optical waveguide.

23. The package of claim 22, wherein the at least one optical waveguide is an optical fiber.

24. A hermetic chip-scale package comprising:

a first housing;

an integrated circuit mounted within said first housing;

a window situated on said first housing; and

wherein:

said integrated circuit has at least one photonic device; and

said first housing and window form a hermetically sealed enclosure around said integrated circuit.

25. The package of claim 24, wherein said window comprises at least one conductive trace connected to said integrated circuit.

26. The package of claim 25, comprising a conductor connected to the at least one conductive trace, for providing a connection external to the hermetically sealed enclosure.

27. The package of claim 26, further comprising a receptacle having said window situated at an end of said receptacle, wherein said receptacle has at least one alignment feature.

26. The package of claim 25, further comprising a plug having an at least one optical waveguide, wherein said plug fits into said receptacle and is aligned with the at least one alignment feature such that one end of the at least one optical waveguide is appropriately proximate to said window.

27. The package of claim 26, wherein the one end of the at least one optical waveguide is aligned with the at least one photonic device.

28. The package of claim 27, further comprising at least one pin securing said plug in said receptacle.

29. The package of claim 28, wherein the at least one photonic device is a VCSEL.

30. The package of claim 29, wherein:
said first housing is composed of ceramic; and
said window is composed of quartz.

31. A chip-scale package for electronic devices, comprising:
a transparent window having at least one conductive trace patterned on a surface of said window;
a semiconductor chip fixed on said window having at least one terminal connected to the at least one conductive trace;
an enclosure surrounding said chip and affixed to said window; and
a conductive path from the at least conductive trace to an at least one pad on an external surface of said enclosure.

32. The package of claim 31, wherein said chip comprises a photonic device.

33. The package of claim 32, wherein said window has at least one feature on the surface of said window for alignment.

34. The package of claim 32, wherein the conductive path is partially embedded in said enclosure.

35. The package of claim 34, wherein the conductive path is connected to a pad on the external surface of said enclosure.

36. The package of claim 35, wherein said enclosure has at least one pad connected to the at least one said conductive trace on said window.

37. The package of claim 36, wherein said enclosure is sealed to said window at a periphery of said window.

38. The package of claim 37, wherein said enclosure is sealed to said window at the periphery of said window by a solder-type material.

39. The package of claim 37, wherein said enclosure is sealed to said window at the periphery of said window by an adhesive-type material.

40. The package of claim 37, wherein said chip is hermetically sealed by said window and enclosure.

41. The package of claim 37, wherein said chip is environmentally sealed by said window and enclosure.

42. The package of claim 40, wherein said window has at least one refractive optical element on the surface of said window.

43. The package of claim 41, wherein said window has at least one refractive optical element on the surface of said window.

44. The package of claim 40, wherein said window has at least one diffractive optical element on the surface of said window.

45. The package of claim 41, wherein said window has at least one diffractive optical element on the surface of said window.

46. The package of claim 33, further comprising a housing attached to said enclosure.

47. The package of claim 46, wherein said housing is mechanically registered to said enclosure by at least one feature on the surface of said window.

48. The package of claim 47, further comprising a ferrule having at least one optical waveguide.

49. The package of claim 48, wherein the at least one optical waveguide is proximate to said window so that light from the waveguide can pass through said window to the at least one photonic device, and so that light from the photonic device can go through said window and to the at least one optical waveguide.

50. The package of claim 49, wherein said window has at least one lens situated between the at least one photonic device and optical waveguide.

51. The package of claim 50, wherein the at least one optical waveguide is an optical fiber.

52. The package of claim 49, further comprising at least one pin securing said ferrule to said enclosure.

53. The package of claim 32, wherein the at least one photonic device is a VCSEL.

54. The package of claim 31, wherein said enclosure comprises ceramic.

55. The package of claim 31, wherein said window comprises quartz.

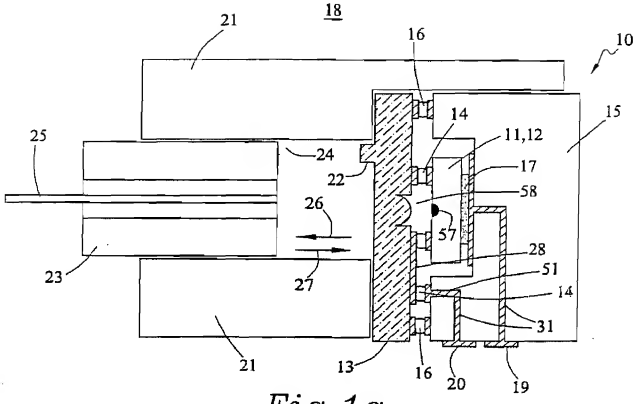
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Fig. 1a

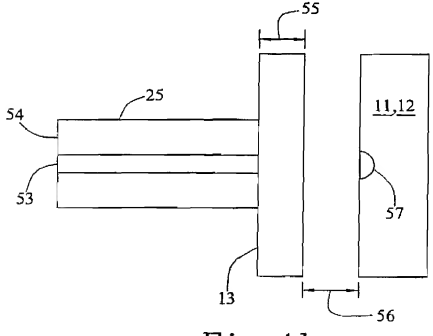
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Fig. 1b

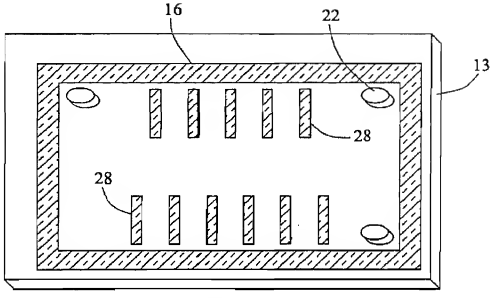


Fig.2a

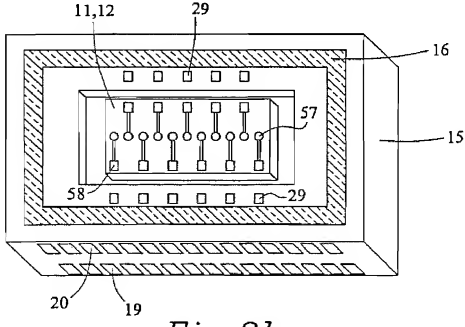


Fig.2b

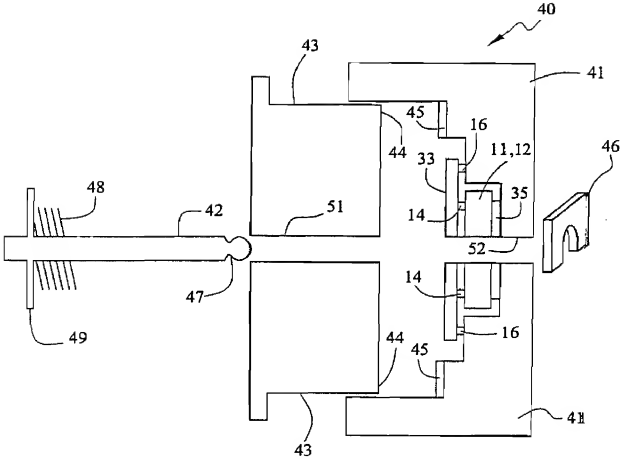


*Fig. 3a*

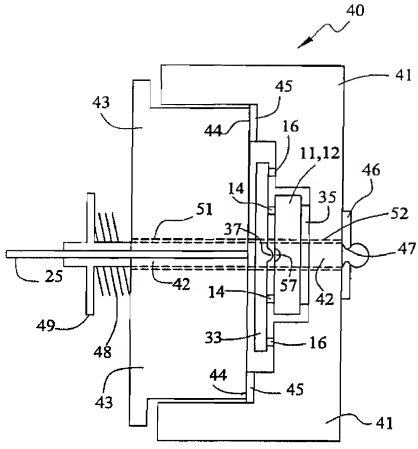


Fig. 3b

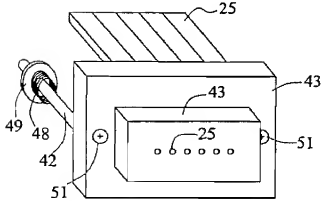


Fig. 4a

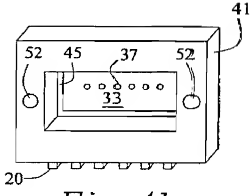


Fig. 4b

# INTERNATIONAL SEARCH REPORT

Interna tal Application No
PCT/US 00/18004

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/0203 H01L33/00 //G02B6/42

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
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